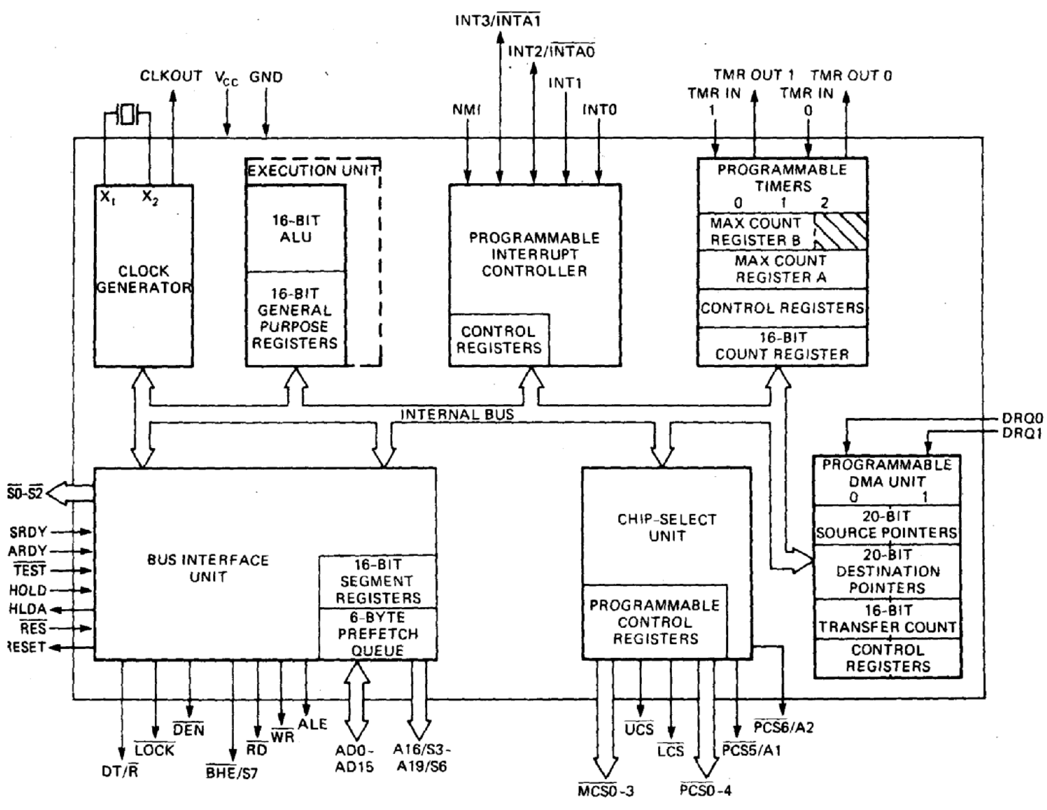
## Intel 80186

80186 contain a 16-bit data bus. The internal register structure of the 80186 is virtually identical to the 8086. The only difference is that the 80186 contain additional reserved interrupt vectors and some very powerful built in I/O features. The 80186 and 80188 are often called embedded controllers because of their application as a controller, not as a microprocessor-based computer.

## Features

- The 80186 contains 16 bit data bus.
- The internal register structure of 80186 is virtually identical to the 8086.
- Enhanced 8086-2 CPU.
- Clock Generator.
- 2 Independent DMA Channels.
- Programmable Interrupt Controller.
- 3 Programmable 16-bit Timers.
- Programmable Memory and Peripheral Chip-Select Logic.
- Available in 10 MHz and 8 MHz Versions.
- Direct Addressing Capability to 1 Mbyte of Memory and 64 Kbyte I/O.

## Architecture



In addition to the BIU and EU, the 80186 family contains a clock generator, a programmable interrupt controller, programmable timers, a programmable DMA controller and a programmable chip selection unit. These enhancements greatly increase the utility of the 80186 and reduce the number of peripheral components required to implement a system.

**Clock Generator.** The internal clock generator replaces the external 8284A clock generator used with the 8086/8088 microprocessors. This reduces the component count in a system. The internal clock generator has three pin connections: X1, X2, and CLKOUT. The X1 (CLKIN) and X2 (OSCOUT) pins are connected to a crystal that resonates at twice the operating frequency of the microprocessor. The CLKOUT pin provides a system clock signal that is one half the crystal frequency. The CLKOUT pin drives other devices in a system and provides a timing source to additional microprocessors in the system.

**Programmable Interrupt Controller.** The programmable interrupt controller (PIC) arbitrates the internal and external interrupts and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function as the master and the 8259 functions as the slave. If the PIC is operated without the external 8259, it has five interrupt inputs: INT0–INT3 and NMI.

**Timers.** The timer section contains three fully programmable l6-bit timers. Timers 0 and 1 generate waveforms for external use and are driven by either the master clock of the 80186 or by an external clock. They are also used to count external events. The third timer, timer 2, is internal and clocked by the master clock. The output of timer 2 generates an interrupt after a specified number of clocks and can provide a clock to the other timers.

**Programmable DMA Unit.** The programmable DMA unit contains two DMA channels or four DMA channels in some models. Each channel can transfer data between memory locations, between memory and I/O, or between I/O devices.

**Programmable Chip Selection Unit.** The chip selection is a built-in programmable memory and I/O decoder. It has six output lines to select memory, seven lines to select I/O on some models, and 10 lines that select either memory or I/O on the some other models.

**Power Save/Power Down Feature.** The power save feature allows the system clock to be divided by 4, 8, or 16 to reduce power consumption. The power-saving feature is started by software and exited by a hardware event such as an interrupt. The power down feature stops the clock completely. The power down mode is entered by execution of an HLT instruction and is exited by any interrupt.

**Refresh Control Unit.** The refresh control unit generates the refresh row address at the interval programmed. The refresh control unit does not multiplex the address for the DRAM—this is still the responsibility of the system designer. The refresh address is provided to the memory system at the end of the programmed refresh interval, along with the control signal. The memory system must run a refresh cycle during the active time of the control signal.

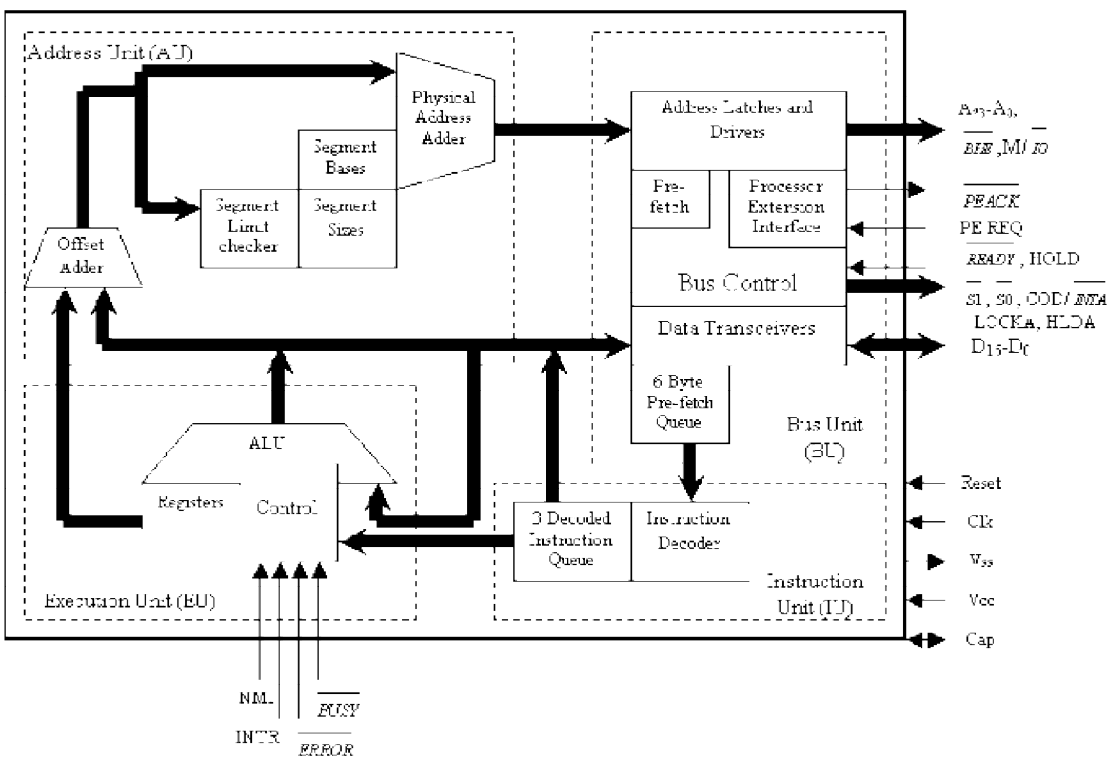
**Intel 80286**

The 80286 is the first member of the family of advanced microprocessors with memory management and protection abilities.

**Features**

- The 80286 microprocessor is an advanced version of the 8086 microprocessor that is designed for multi user and multitasking environments.
- The 80286 addresses 16 M Byte of physical memory and 1G Bytes of virtual memory by using its memory-management system.
- The 80286 is basically an 8086 that is optimized to execute instructions in fewer clocking periods than the 8086.
- Various versions of 80286 are available that runs on 12.5 MHz , 10 MHz and 8 MHz clock frequencies.
- Like the 80186, the 80286 doesn't incorporate internal peripherals; instead it contains a memory management unit (MMU).
- The 80286 operates in both the real and protected modes
- In the real mode, the 80286 addresses a 1MByte memory address space and is virtually identical to 8086.
- In the protected mode, the 80286 addresses a 16MByte memory space.

**Architecture**



The CPU contain four functional blocks
1. Address Unit (AU)
2. Bus Init (BU)
3. Instruction Unit (IU)
4.Execution Unit (EU)

**Address Unit:** The address unit is responsible for calculating the physical address of instructions and data that the CPU wants to access. Also the address lines derived by this unit may be used to address different peripherals. The physical address computed by the address unit is handed over to the bus unit (BU) of the CPU.

**Bus Unit:** Major function of the bus unit is to fetch instruction bytes from the memory. Instructions are fetched in advance and stored in a queue to enable faster execution of the instructions. The bus unit also contains a bus control module that controls the prefetcher module. These prefetched instructions are arranged in a 6-byte instructions queue. The 6-byte prefetch queue forwards the instructions arranged in it to the instruction unit(IU).

**Instruction Unit:** The instruction unit(IU) accepts instructions from the prefetch queue and an instruction decoder decodes them one by one. The decoded instructions are latched onto a decoded instruction queue. The output of the decoding circuit drives a control circuit in the execution unit.

**Execution Unit:** The execution unit(EU) is responsible for executing the instructions received from decoded instruction queue. The decoded instruction queue sends the data part of the instruction over the data bus. The EU contains the register bank used for storing the data as scratch pad, or used as special purpose registers. The ALU, the heart of the EU, carries out all the arithmetic and logical operations and sends the results over the data bus or back to the register bank.

**Register Organization of 80286**

The 80286 CPU contains almost the same set of registers, as in 8086, namely
1. Eight 16-bit general purpose registers
2. Four 16-bit segment registers
3. Status and control registers
4. Instruction Pointer

The flag register reflects the results of logical and arithmetic instructions.

| - | NT | IOPL | OF | DF | IF | TF | SF | ZF | - | AF | - | PF | - | CF |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | |

$D_2$, $D_4$, $D_6$, $D_7$ and $D_{11}$ are called as status flag bits. The bits $D_8$ (TF) and $D_9$ (IF) are used for controlling machine operation and thus they are called control flags. The additional fields available in 80286 flag registers are :

1. **IOPL - I/O Privilege Field** (bits D12 and D13)

2. **NT - Nested Task flag** (bit D14)

3.**PE - Protection Enable** (bit D16, is set to select the protected mode of operation. The 80286 could not return to real mode without a hardware reset)

4. **MP - Monitor Processor Extension** (bit D17, is set to indicate that the arithmetic coprocessor is present in the system)

5. **EM - Processor Extension Emulator** (bit D18, Is set to cause a type 7 interrupt for each ESC instruction. We often use this interrupt to emulate, with software, the function of the coprocessor. Emulation reduces the system cost, but it often requires at least 100 times longer to execute the emulated coprocessor instructions.)

6. **TS – Task Switch** (bit D19, If TS = 1, a numeric coprocessor instruction causes a type 7 (coprocessor not available) interrupt.)

**Machine Status Word (MSW)**

The machine status word consists of four flags – PE, MP, EM and TS of the four lower order bits D19 to D16 of the upper word of the flag register. The LMSW and SMSW instructions are available in the instruction set of 80286 to write and read the MSW in real address mode.

**Real Address Mode**

• Act as a fast 8086

• Instruction set is upwardly compatible

• It address only 1 M byte of physical memory using A0-A19.

• In real addressing mode of operation of 80286, it just acts as a fast 8086. The instruction set is upward compatible with that of 8086.

The 80286 addresses only 1Mbytes of physical memory using A0- A19. The lines A20-A23 are not used by the internal circuit of 80286 in this mode. In real address mode, while addressing the physical memory, the 80286 uses BHE along with A0- A19. The 20-bit physical address is again formed in the same way as that in 8086. The contents of segment registers are used as segment base addresses.

As in 8086, the physical memory is organized in terms of segments of 64Kbyte maximum size. An exception is generated, if the segment size limit is exceeded by the instruction or the data. The overlapping of physical memory segments is allowed to minimize the memory requirements for a task. The 80286 reserves two fixed areas of physical memory for system initialization and interrupt vector table. In the real mode the first 1Kbyte of memory starting from address 0000H to 003FFH is reserved for interrupt vector table.

Also the addresses from FFFF0H to FFFFFH are reserved for system initialization. The program execution starts from FFFFH after reset and initialization. The interrupt vector table of 80286 is organized in the same way as that of 8086. Some of the interrupt types are reserved for exceptions, single-stepping and processor extension segment overrun, etc. When the 80286 is reset, it always starts the execution in real address mode.

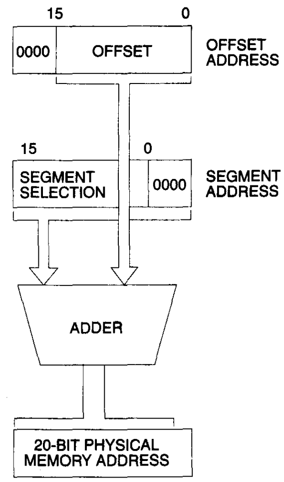



**Fig: Real address mode Address calculation**

**PROTECTED VIRTUAL ADDRESS MODE (PVAM)**

80286 is the first processor to support the concepts of virtual memory and memory management. The virtual memory does not exist physically it still appears to be available within the system. The concept of VM is implemented using Physical memory that the CPU can directly access and secondary memory that is used as a storage for data and program, which are stored in secondary memory initially.

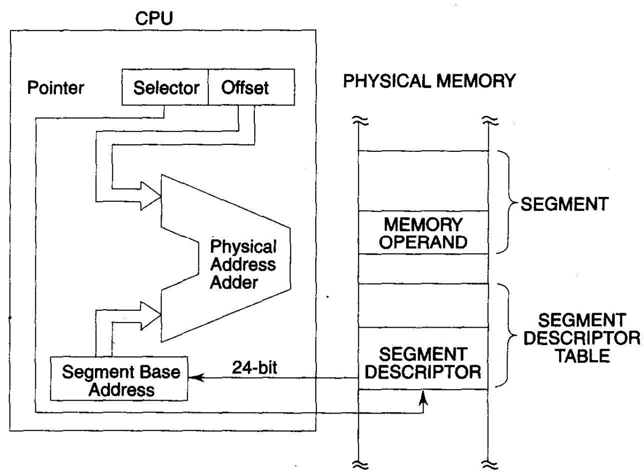
The Segment of the program or data required for actual execution at that instant, is fetched from the secondary memory into physical memory. After the execution of this fetched segment, the next segment required for further execution is again fetched from the secondary memory, while the results of the executed segment are stored back into the secondary memory for further references. This continues till the complete program is executed.

During the execution the partial results of the previously executed portions are again fetched into the physical memory, if required for further execution. The procedure of fetching the chosen program segments or data from the secondary storage into physical memory is called *swapping*. The procedure of storing back the partial results or data back on the secondary storage is called *unswapping*. The virtual memory is allotted per task.

The 80286 is able to address 1 G byte (230 bytes) of virtual memory per task. The complete virtual memory is mapped on to the 16Mbyte physical memory. If a program larger than 16Mbyte is stored on the hard disk and is to be executed , if it is fetched in terms of data or program segments of less than 16Mbyte in size into the program memory by swapping sequentially as per sequence of execution.

Whenever the portion of a program is required for execution by the CPU, it is fetched from the secondary memory and placed in the physical memory is called *swapping in* of the program. A portion of the program or important partial results required for further execution, may be saved back on secondary storage to make the PM free for further execution of another required portion of the program is called *swapping out* of the executable program.

80286 uses the 16-bit content of a segment register as a selector to address a descriptor stored in the physical memory. The descriptor is a block of contiguous memory locations containing information of a segment, like segment base address, segment limit, segment type, privilege level, segment availability in physical memory, descriptor type and segment use another task.



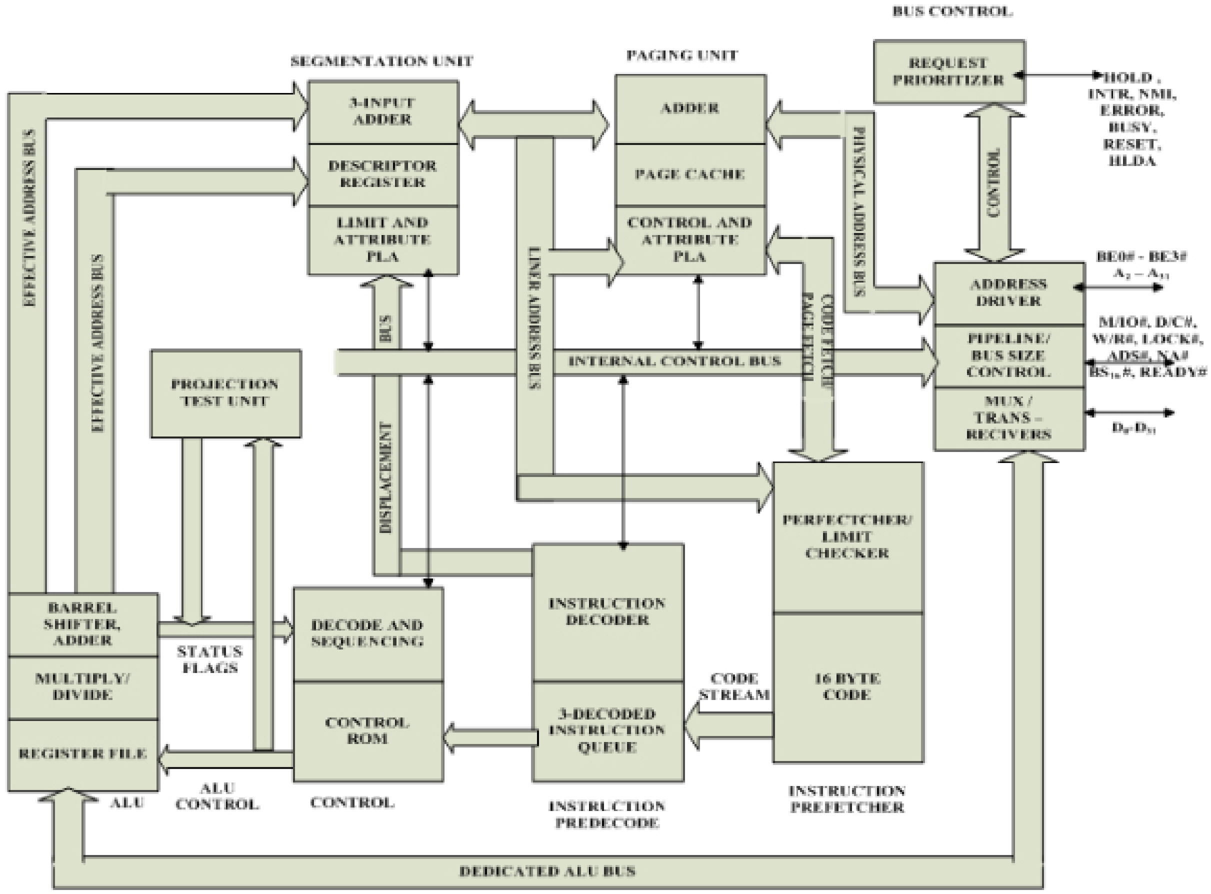

**Physical address calculation in PVAM**

**Intel 80386**

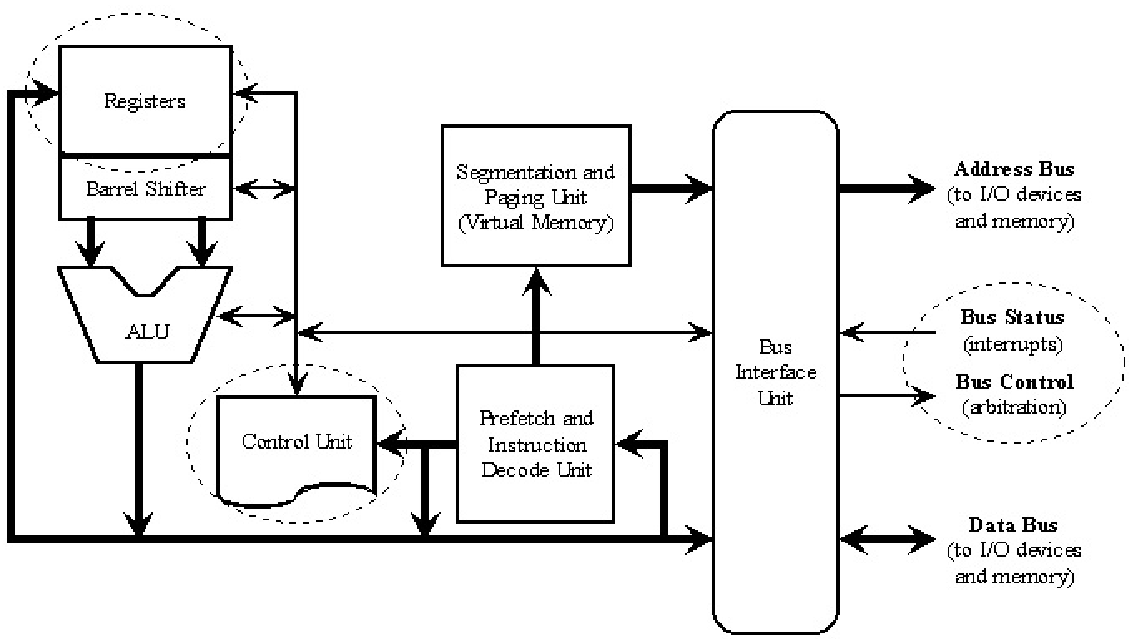
**Features**

- 32-bit general and offset registers.
- 16-byte prefetch queue.
- Memory Management Unit with a Segmentation Unit and a Paging Uni.t
- 32-bit Address and Data Bus.
- 4-Gbyte Physical address space.
- 64-Tbyte virtual address space.
- i387 numerical coprocessor with IEEE standard-754-1985 for floating point arithmetic.
- 64K 8-, 16-, or 32-bit ports.
- Implementation of real, protected and virtual 8086 modes.
- The protection mode opeartion provides paging,virtual addressing,multilevel protection and multitasking capabilities.

**Architecture**




OR



The Internal Architecture of 80386 is divided into 3 sections.
•Central processing unit
•Memory management unit
•Bus interface unit

**Central processing unit** is further divided into Execution unit and Instruction unit. **Execution unit** has 8 General purpose and 8 Special purpose registers which are either used for handling data or calculating offset addresses. The **Instruction unit** decodes the opcode bytes received from the 16-byte instruction code queue and arranges them in a 3- instruction decoded instruction queue.After decoding them pass it to the control section for deriving the necessary control signals.

• The **barrel shifter** increases the speed of all shift and rotate operations.

• The **multiply / divide logic** implements the bit-shift-rotate algorithms to complete the operations in minimum time.Even 32- bit multiplications can be executed within one microsecond by the multiply /divide logic.

•The **Memory management unit** consists of a Segmentation unit and a Paging unit.

•**Segmentation unit** allows the use of two address components, viz. segment and offset for relocability and sharing of code and data. Segmentation unit allows segments of size 4Gbytes at max. The Segmentation unit provides a 4 level protection mechanism for protecting and isolating the system code and data from those of the application program.

•The **Paging unit** organizes the physical memory in terms of pages of 4kbytes size each. Paging unit works under the control of the segmentation unit, i.e. each segment is further divided into pages. The virtual memory is also organizes in terms of segments and pages by the memory management unit. Paging unit converts linear addresses into physical addresses. The advantage of paging scheme is that the complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Thus the memory requirement of the task is substantially reduced, relinquishing the available memory for other tasks. Whenever the other pages of task are required for execution, they may be fetched from the secondary storage. The previous page which are executed, need not be available in the memory, and hence the space occupied by them may be relinquished for other tasks. Thus paging mechanism provides an effective technique to manage the physical memory for multitasking systems.

•The **control and attribute PLA** checks the privileges at the page level. Each of the pages maintains the paging information of the task. The limit and attribute PLA checks segment limits and attributes at segment level to avoid invalid accesses to code and data in the memory segments.

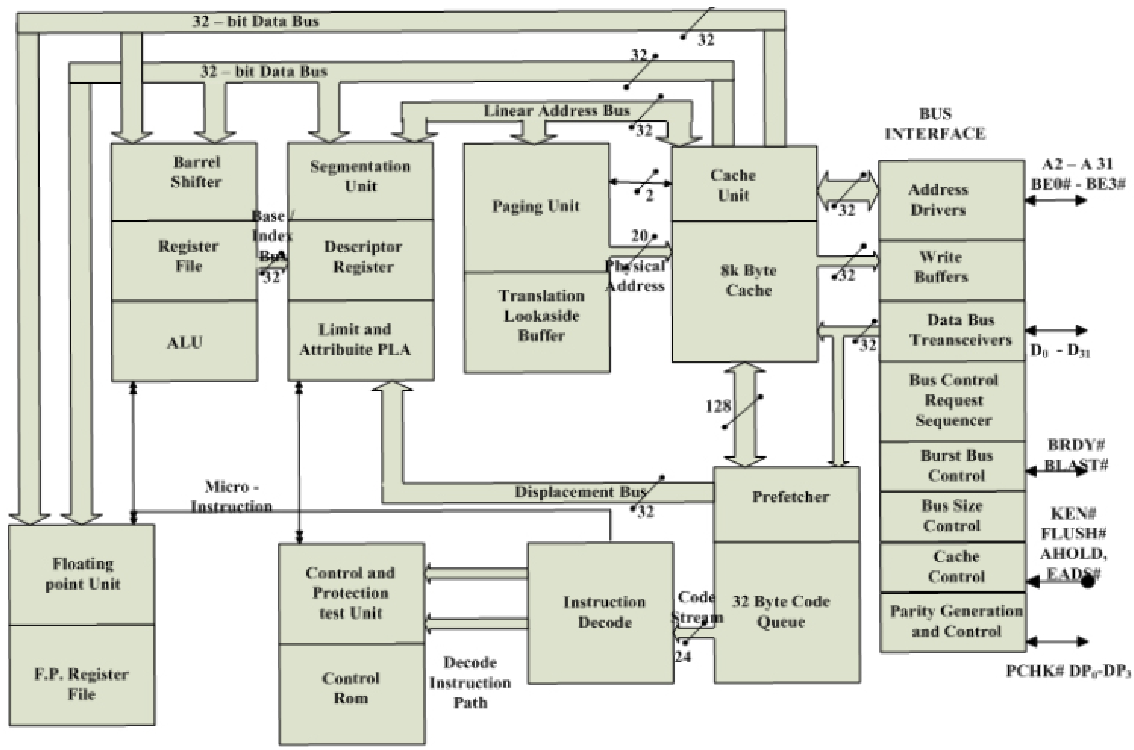
•The **Bus control unit** has a prioritizer to resolve the priority of the various bus requests. This controls the access of the bus. The address driver drives the bus enable and address signal A0 – A31. The pipeline and dynamic bus sizing unit handle the related control signals.

•The **data buffers** interface the internal data bus with the system bus.

**Intel 80486**

**Features**

- Improved 80386 CPU (6 extra instructions)
- Hard-wired implementation of frequently used instructions (as in RISCs)
- A 5 stage instruction pipeline
- An 8K Cache Memory + cache controller (previously a separate device)
- An on-chip Floating Point coprocessor
- Longer Prefetch Queue (32-bytes as opposed to 16 on the 80386)
- Higher frequency operation
- About a million transistors
- Like the 80386 it uses real, protected and virtual 8086 modes and its Memory Management Unit include a Segmentation Unit and a Paging Unit.




**The Pentium Processors**

The Pentium microprocessor signals an improvement to the architecture found in the 80486 microprocessor. The changes include an improved cache structure, a wider data bus width, a faster numeric coprocessor, a dual integer processor, and branch prediction logic. The cache has been reorganized to form two caches that are each 8K bytes in size, one for caching data, and the other for instructions. The data bus width has been increased from 32 bits to 64 bits. The numeric coprocessor operates at about five times faster than the 80486 numeric coprocessor. A dual-integer processor often allows two instructions per clock. Finally, the branch prediction logic allows programs that branch to execute more efficiently.

**Features of Pentium Processors:**

- It is a highly integrated device containing about 1.2 million transistors.
- **Wider Data Bus Width:** The Pentium processors have a wider data bus width. The data bus width has been increased from 32-bit to 64-bit to improve the data transfer rate.
- **Faster Floating Point Unit:** Faster algorithm provides up to ten times speed-up for common operations including add, multiply and load.
- **Improved Cache Structure:** Pentium processors include separate code and data caches integrated on-chip to meet performance goals.
- **Dual Integer Processor:** Pentium processor has integer processor. It allows execution of two instructions per clock.
- **Branch Prediction Logic:** The Pentium uses the technique called branch prediction to check whether a branch will be valid or invalid.
- **Data Integrity and Error Detection:** The Pentium processors have added significant data integrity and error detection capability.
- **Super Scalar Processor:** Processors capable to parallel instruction execution of multiple instructions are known as super scalar processors. The Pentium is capable, under special circumstances of executing two integer or two floating point instructions simultaneously and thus it support super scalar architecture.

The Pentium MMX version contained an additional MMX unit that speeds up multimedia and 3D applications. Processing multimedia data involved instructions operating on large volumes of packetized data.

**Salient Features Of 80586 (Pentium)**

A salient feature of Pentium is its superscalar, super pipelined architecture. It has two integer pipelines U and V, where each one is a 4-stage pipeline. This enhances the speed of integer arithmetic of Pentium to a large extent. Moreover, it has an on-chip floating-point unit, which has increased the floating-point performance manifold compared to the floating- point performances of 80386/486 processors.

Another feature of Pentium is that it contains two separate caches, viz. data cache and instruction cache. In 80486 there was a single unified data/instruction cache.

The Intel CPU architectures up to 80486 issues only one instruction to the execution unit per cycle. This obviously leads to a comparatively slow process of decoding and execution. For enhancement of processor performance beyond one instruction per cycle, the computer architects employ the technique of multiple instruction issue (MII). Thus a microprocessor which is capable of issuing more thaw instruction per single processor cycle will be termed as MII microprocessor. Obvious executing more than one instruction in a cycle, the microprocessor must have more than execution channels.

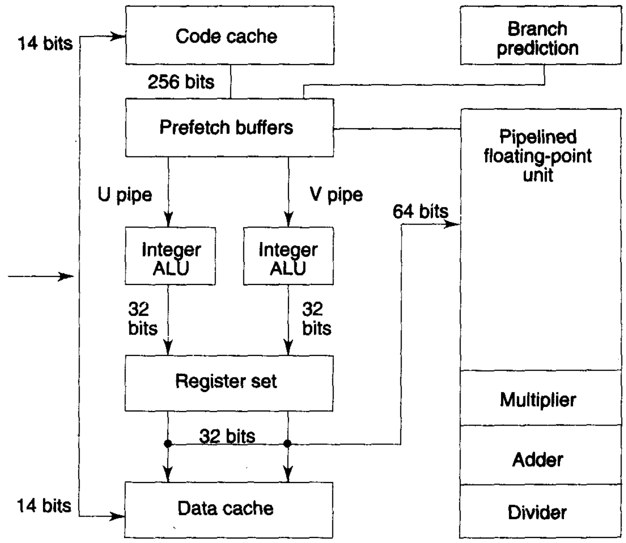



**Fig. 5 .1 Pentium CPU Architecture**

**Pentium II**

Pentium II is also a 32-bit processor with 64-bit data bus and 36-bit address bus to address up to 64GB of physical memory space. It is actually a Pentium pro processor with on-chip MMX (Multi Media Extension). It is available with maximum internal ratings of 233 MHz to 450 MHz.

The features of Pentium II processor are;

(i) Supports the INTEL architecture with dynamic execution.
(ii) Integrated primary (L1) 16-kb instruction cache and 16-kb write back data cache.
(iii) Integrated 256kb second level (L2) cache.
(iv) Fully compatible with previous microprocessors.
(v) Supports MMX technology.
(vi) Quick start and Deep sleep modes provide extremely low power dissipation.
(vii) Integrated math co-processor.

**The Pentium III**

The Pentium III microprocessor is an improved version of the Pentium II microprocessor. Even though it is newer than the Pentium II, it is still based on the Pentium Pro architecture.

The salient architectural features are:

1. P-III CPU has been developed using 0.25 micron technology and includes over 9.5 million transistors. It has three versions operating at 450 MHz, 500 MHz and 550 MHz which are commercially available.
2. P-III incorporates multiple branch prediction algorithms.

3. Seventy new instructions have been added to Pentium III. These instructions are useful in advanced imaging, speech processing and multimedia applications.
4. Dual independent bus architecture increases bandwidth.
5. P-III employs dynamic execution technology.
6. A 512Kbyte unified, non-blocking level 2 cache has been used.
7. Eight 64-bit wide Intel MMX registers along with a set of 57 instructions for multimedia applications are available

**Pentium IV**

The most recent version of the Pentium Pro architecture microprocessor is the Pentium 4 microprocessor from Intel. The Pentium 4 was released initially in November 2000 with a speed of 1.3 GHz. It is currently available in speeds up to 2.0 GHz. There are two packages available for this integrated microprocessor, the 423-pin PGA and the 478-pin FC-PGA2. Both versions use the 1.8 micron technology for fabrication. As with earlier versions of the Pentium, the Pentium 4 uses a 100-MHz memory bus speed.

**Comparison Between different Processors**

| Name | Date | Internal Reg: | Clock Speed | Data Width | Address Lines | Max: Memory Space |
|---|---|---|---|---|---|---|
| 8086 | 1974 | 16 Bit | 2 MHZ | 16 bits | 20 Bit | 1MB |
| 80286 | 1982 | 16 Bit | 6 MHZ | 16 bits | 24 Bit | 16 MB |
| 80386 | 1985 | 32 Bit | 16 MHZ | 32 bits | 32 Bit | 4 GB |
| 80486 | 1989 | 32 Bit | 25 MHZ | 32 bits | 32 Bit | 4 GB |
| Pentium | 1993 | 32 Bit | 60 MHZ | 32 bits, 64 bit bus | 32 Bit | 4 GB |
| Pentium II | 1997 | 32 Bit | 233 MHZ | 32 bits, 64 bit bus | 32 Bit | 64 GB |
| Penium III | 1999 | 32 Bit | 450 MHZ | 32 bits , 64 bit bus | 32 Bit | 64 GB |
| Pentium IV | 2000 | 32 Bit | 1.5 MHZ | 32 bits, 64 bit bus | 32 Bit | 64 GB |